

wherein said gate electrode includes:

a silicon film formed on said gate insulating film,

a silicide film formed on a surface of said silicon film,

second side walls ON inner walls of said first side walls,

a plane portion held between said second side walls, and

said silicide film has a smaller thickness than a height of said second

side walls from said plane portion.

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cont'd.

REMARKS

Favorable reconsideration of this application, as presently amended, is respectfully requested.

Claims 10-13 are pending in this application. Claim 10 was rejected under 35 U.S.C. § 102(e) as anticipated by U.S. patent 5,877,085 to Matsubara. Claim 11 was rejected under 35 U.S.C. § 103(a) as unpatentable over Matsubara in view of U.S. patent 5,554,566 to Lur et al. (herein "Lur"). Claim 12 was rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. patent 5,702,986 to Mathews et al. (herein "Mathews") in view of U.S. patent 5,656,519 to Mogami. Claim 13 was rejected under 35 U.S.C. § 103(a) as unpatentable over Mathews in view of Mogami and further in view of Lur.

Addressing the above-noted rejection of Claim 10 under 35 U.S.C. § 102(e) as anticipated by Matsubara, and the rejection of Claim 11 under 35 U.S.C. § 103(a) as unpatentable over Matsubara in view of Lur, those rejections are traversed by the present response.

It is initially noted that Claim 1 is amended by the present response to clarify the formation of a structure of "said gate electrode" and to clarify that "said substrate silicide

film has a smaller thickness than a height of said second side walls from said plane portion”. That subject matter is fully supported by the original specification for example in Figure 29 as a non-limiting example. As shown in the non-limiting example of Figure 29 the height of the side wall 44 is greater than the thickness of the silicide film 45. Further, the specification indicates at page 22, line 17, to page 23, line 1, that such a structure “serves as increase of the widths of the silicide films 45”. As also discussed in the specification, the silicide can be substantially lengthened due to the side wall 44, thereby causing the phase transition thereof and reducing gate resistance.

Such a structure as clarified in the claims is believed to also distinguish over the applied art to Matsubara, and further in view of Lur.

In Figure 4G Matsubara shows a silicide layer 112 having a protrusion at a portion adjacent to a spacer 105. However, in Matsubara that protrusion is not positively formed and has a height *smaller* than the thickness of the silicide layer 112.

As a result, the device of Matsubara cannot achieve the advantageous effects of extending a silicide layer on a gate to be longer than the gate length. Further, Matsubara fails to teach or suggest problems such as phase transition, which the invention of Claims 10 and 11 can address.

According to Claims 10 and 11, due to the side wall having a height greater than the thickness of the silicide film, the silicide film can be extended longer than the gate length, thereby reducing gate resistance. Such a feature is not taught, nor suggested, nor possible in the devices of Matsubara or Lur.

In such ways, Claims 10 and 11 are believed to clearly distinguish over the applied art.

With respect to the rejection of Claim 12 under 35 U.S.C. § 103(a) as unpatentable

over Mathews in view of Mogami, and the rejection of Claim 13 further in view of Lur, those rejections are also traversed by the present response.

It is respectfully submitted that there is no incentive or motivation to one of ordinary skill in the art to modify Mathews to meet the claim limitations.

- As recognized in the Office Action, "Mathews et al. does not teach that source/drain regions have a silicified surface".²

To overcome the recognized deficiencies in Mathews the outstanding Office Action cites the teachings in Mogami, and in particular Mogami disclosing source/drain regions 10, 11 having silicified surfaces 13b in Figure 5F. However, it is respectfully submitted that such teachings in Mogami are not properly applicable to the teachings in Mathews.

In Mathews the surface of the polycrystalline silicon layer 11 which is to become a gate electrode is silicified to provide layer 12 *before* doping source/drain impurities. As a result, in Mathews there can be clearly no incentive or motivation to silicify the surface of source/drain regions 44, in contrast to the claims.

Further, as discussed in the present specification, for example with respect to Figure 42 and at page 26, line 5 et seq. as an example, the silicide films 56 are formed on surfaces of both the gate electrode 5 and the high-concentration source/drains 8; i.e. that operation as shown in Figure 42 takes place in the same step.

As Mathews does not even disclose or suggest forming the source/drain regions 44 prior to forming the layer 12 on the silicon layer 11, Mathews clearly cannot teach or suggest silicifying such source/drain regions 44.

Stated another way, if it was at all desirable to silicify the source/drain regions 44 in the device of Mathews, then Mathews at the very least would have to form those source/drain

²Office Action of January 10, 2003, page 4, line 11.

regions 44 prior to the forming the layer 12, i.e. Mathews would have to dope the regions to form the source/drain areas 44 prior to the silicifying step. Mathews fails to teach or suggest such an operation. Thereby, one of ordinary skill in the art would not modify Mathews to form an additional silicifying step after already providing the layer 12.

Moreover, Mogami does not teach or suggest a step in which a silicon layer, such as layer 11 in Mathews, would be silicified at a different time than source/drain regions.

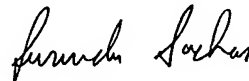
Thereby, the teachings in Mogami are not properly applicable to the teachings in Mathews.

In such ways, no combination of teachings of Mathews in view of Mogami renders obvious Claims 12 and 13 as currently written. Moreover, no teachings in Lur can overcome the above-noted deficiencies of Mathews in view of Mogami.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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IN THE CLAIMS

10. (Twice Amended) A MIS transistor including:

a gate electrode being formed to be opposed to a silicon substrate through a gate insulating film;

first side walls being insulative and formed on said silicon substrate on both sides of said gate electrode, said first side walls being higher than said gate electrode from said silicon substrate; [and]

[a silicon film being formed on walls closer to said gate electrode to be connected with said gate electrode, a surface of said silicon film, together with said gate electrode, being silicified and forming a concave portion a silicon film being formed on walls closer to said gate electrode to be connected with said gate electrode, a surface of said silicon film, together with said gate electrode, being silicified and forming a concave portion]

wherein said gate electrode includes:

a silicon film formed on said gate insulating film,

a silicide film formed on a surface of said silicon film,

second side walls on inner walls of said first side walls,

a plane portion held between said second side walls, and

said silicide film has a smaller thickness than a height of said second side walls from said plane portion.